# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

# 74HC/HCT193
## Presettable synchronous 4-bit binary up/down counter

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

# Presettable synchronous 4-bit binary up/down counter

# 74HC/HCT193

## FEATURES

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard
- $I_{CC}$ category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT193 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT193 are 4-bit synchronous binary up/down counters. Separate up/down clocks, $CP_U$ and $CP_D$ respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the $CP_U$ clock is pulsed while $CP_D$ is held HIGH, the device will count up. If the $CP_D$ clock is pulsed while $CP_U$ is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$).

The "193" contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the $CP_D$ input will decrease the count by one, while a similar transition on the $CP_U$ input will advance the count by one.

One clock should be held HIGH while counting with the other, otherwise the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up ($\overline{TC}_U$) and terminal count down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of $CP_U$ will cause $\overline{TC}_U$ to go LOW.

$\overline{TC}_U$ will stay LOW until $CP_U$ goes HIGH again, duplicating the count up clock.

Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the $CP_D$ goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs ($D_0$ to $D_3$) is loaded into the counter and appears on the outputs ($Q_0$ to $Q_3$) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs ($Q_0$ to $Q_3$) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r = t_f$ = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|---|---|---|---|---|---|
| | | | HC | HCT | |
| $t_{PHL}/ t_{PLH}$ | propagation delay $CP_D$, $CP_U$ to $Q_n$ | $C_L$ = 15 pF; $V_{CC}$ = 5 V | 20 | 20 | ns |
| $f_{max}$ | maximum clock frequency | | 45 | 47 | MHz |
| $C_I$ | input capacitance | | 3.5 | 3.5 | pF |
| $C_{PD}$ | power dissipation capacitance per package | notes 1 and 2 | 24 | 26 | pF |

**Notes**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   $f_i$ = input frequency in MHz

   $f_o$ = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   $C_L$ = output load capacitance in pF

   $V_{CC}$ = supply voltage in V

2. For HC the condition is $V_I$ = GND to $V_{CC}$
   For HCT the condition is $V_I$ = GND to $V_{CC}$ − 1.5 V

## ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

## PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 3, 2, 6, 7 | $Q_0$ to $Q_3$ | flip-flop outputs |
| 4 | $CP_D$ | count down clock input(1) |
| 5 | $CP_U$ | count up clock input(1) |
| 8 | GND | ground (0 V) |
| 11 | $\overline{PL}$ | asynchronous parallel load input (active LOW) |
| 12 | $\overline{TC}_U$ | terminal count up (carry) output (active LOW) |
| 13 | $\overline{TC}_D$ | terminal count down (borrow) output (active LOW) |
| 14 | MR | asynchronous master reset input (active HIGH) |
| 15, 1, 10, 9 | $D_0$ to $D_3$ | data inputs |
| 16 | $V_{CC}$ | positive supply voltage |

**Note**

1. LOW-to-HIGH, edge triggered

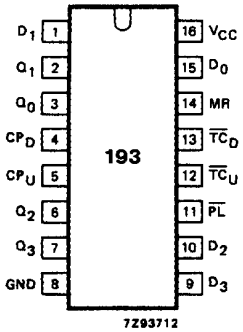


Fig.1 Pin configuration.

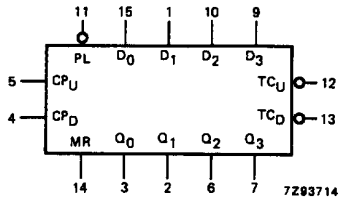


Fig.2 Logic symbol.

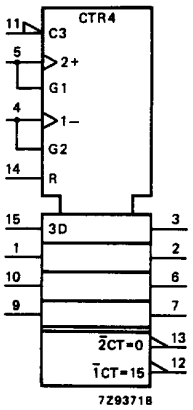


Fig.3 IEC logic symbol.

**FUNCTION TABLE**

| OPERATING MODE | INPUTS | | | | | | | | OUTPUTS | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MR | $\overline{PL}$ | $CP_U$ | $CP_D$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $\overline{TC}_U$ | $\overline{TC}_D$ |
| reset (clear) | H<br>H | X<br>X | X<br>X | L<br>H | X<br>X | X<br>X | X<br>X | X<br>X | L<br>L | L<br>L | L<br>L | L<br>L | H<br>H | L<br>H |
| parallel load | L<br>L<br>L<br>L | L<br>L<br>L<br>L | X<br>X<br>L<br>H | L<br>H<br>X<br>X | L<br>L<br>H<br>H | L<br>L<br>H<br>H | L<br>L<br>H<br>H | L<br>L<br>H<br>H | L<br>L<br>H<br>H | L<br>L<br>H<br>H | L<br>L<br>H<br>H | L<br>L<br>H<br>H | H<br>H<br>L<br>H | L<br>H<br>H<br>H |
| count up | L | H | ↑ | H | X | X | X | X | count up | | | | $H^{(2)}$ | H |
| count down | L | H | H | ↑ | X | X | X | X | count down | | | | H | $H^{(3)}$ |

**Notes**

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH clock transition
2. $\overline{TC}_U = CP_U$ at terminal count up (HHHH)
3. $\overline{TC}_D = CP_D$ at terminal count down (LLLL)

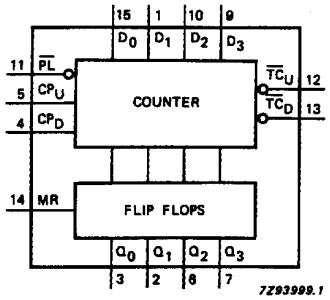


Fig.4 Functional diagram.

(1) Clear overrides load, data and count inputs.

(2) When counting up the count down clock input ($CP_D$) must be HIGH, when counting down the count up clock input ($CP_U$) must be HIGH.

**Sequence**

Clear (reset outputs to zero);

load (preset) to binary thirteen;

count up to fourteen, fifteen, terminal count up, zero, one and two;

count down to one, zero, terminal count down, fifteen,

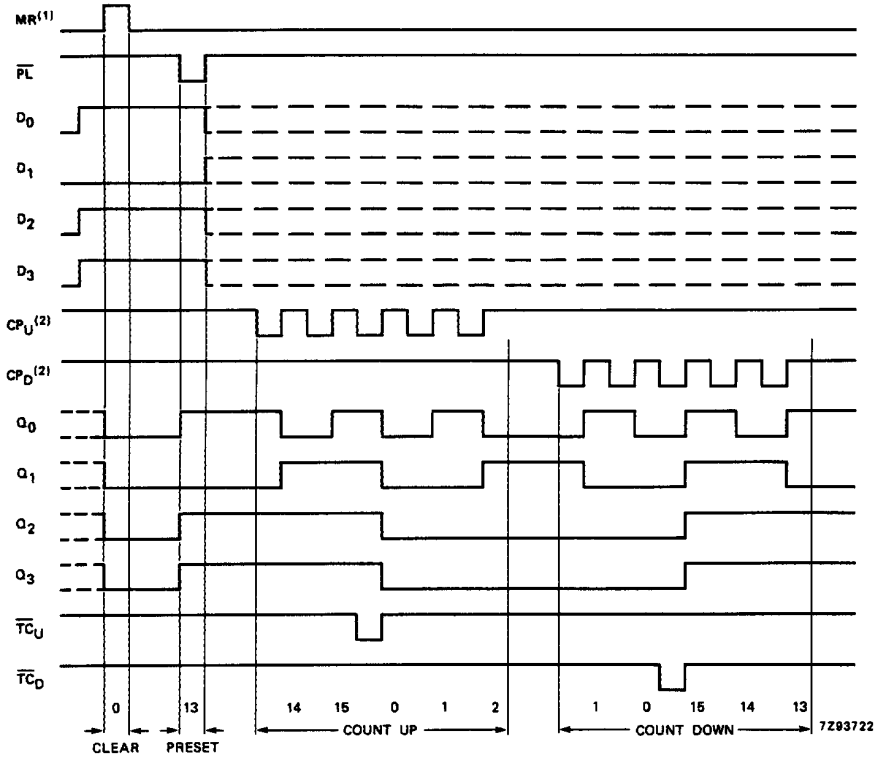


Fig.5 Typical clear, load and count sequence.

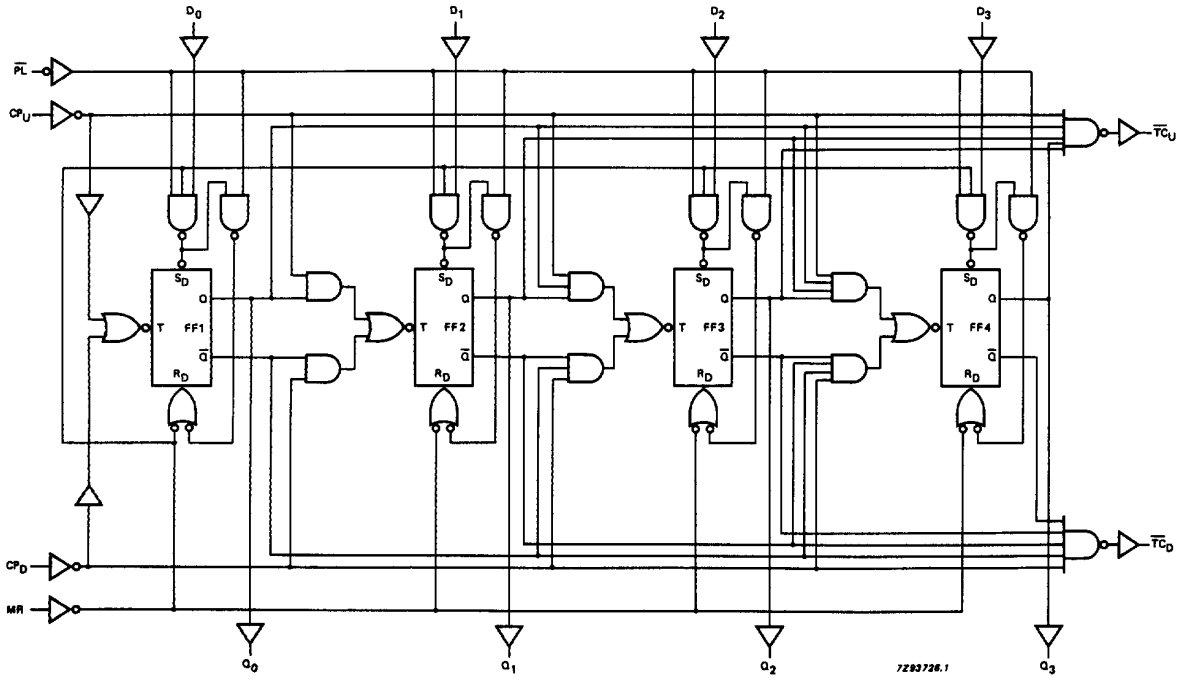


Fig.6 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}/ t_{PLH}$ | propagation delay $CP_U$, $CP_D$ to $Q_n$ | | 63<br>23<br>18 | 215<br>43<br>37 | | 270<br>54<br>46 | | 325<br>65<br>55 | ns | 2.0<br>4.5<br>6.0 | Fig.7 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $CP_U$ to $\overline{TC}_U$ | | 39<br>14<br>11 | 125<br>25<br>21 | | 155<br>31<br>26 | | 190<br>38<br>32 | ns | 2.0<br>4.5<br>6.0 | Fig.8 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $CP_D$ to $\overline{TC}_D$ | | 39<br>14<br>11 | 125<br>25<br>21 | | 155<br>31<br>26 | | 190<br>38<br>32 | ns | 2.0<br>4.5<br>6.0 | Fig.8 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $\overline{PL}$ to $Q_n$ | | 69<br>25<br>20 | 220<br>44<br>37 | | 275<br>55<br>47 | | 330<br>66<br>56 | ns | 2.0<br>4.5<br>6.0 | Fig.9 |
| $t_{PHL}$ | propagation delay MR to $Q_n$ | | 58<br>21<br>17 | 200<br>40<br>34 | | 250<br>50<br>43 | | 300<br>60<br>51 | ns | 2.0<br>4.5<br>6.0 | Fig.10 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $D_n$ to $Q_n$ | | 69<br>25<br>20 | 210<br>42<br>36 | | 265<br>53<br>45 | | 315<br>63<br>54 | ns | 2.0<br>4.5<br>6.0 | Fig.9 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $\overline{PL}$ to $\overline{TC}_U$, $\overline{PL}$ to $\overline{TC}_D$ | | 80<br>29<br>23 | 290<br>58<br>49 | | 365<br>73<br>62 | | 435<br>87<br>74 | ns | 2.0<br>4.5<br>6.0 | Fig.12 |
| $t_{PHL}/ t_{PLH}$ | propagation delay MR to $\overline{TC}_U$, MR to $\overline{TC}_D$ | | 74<br>27<br>22 | 285<br>57<br>48 | | 355<br>71<br>60 | | 430<br>86<br>73 | ns | 2.0<br>4.5<br>6.0 | Fig.12 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $D_n$ to $\overline{TC}_U$, $D_n$ to $\overline{TC}_D$ | | 80<br>29<br>23 | 290<br>58<br>49 | | 365<br>73<br>62 | | 435<br>87<br>74 | ns | 2.0<br>4.5<br>6.0 | Fig.12 |
| $t_{THL}/ t_{TLH}$ | output transition time | | 19<br>7<br>6 | 75<br>15<br>13 | | 95<br>19<br>16 | | 110<br>22<br>19 | ns | 2.0<br>4.5<br>6.0 | Fig.10 |
| $t_W$ | up, down clock pulse width HIGH or LOW | 100<br>20<br>17 | 22<br>8<br>6 | | 125<br>25<br>21 | | 150<br>30<br>26 | | ns | 2.0<br>4.5<br>6.0 | Fig.7 |

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_W$ | master reset pulse width HIGH | 100<br>20<br>17 | 25<br>9<br>7 | | 125<br>25<br>21 | | 150<br>30<br>26 | | ns | 2.0<br>4.5<br>6.0 | Fig.10 |
| $t_W$ | parallel load pulse width LOW | 100<br>20<br>17 | 19<br>7<br>6 | | 125<br>25<br>21 | | 150<br>30<br>26 | | ns | 2.0<br>4.5<br>6.0 | Fig.9 |
| $t_{rem}$ | removal time $\overline{PL}$ to $CP_U$, $CP_D$ | 50<br>10<br>9 | 8<br>3<br>2 | | 65<br>13<br>11 | | 75<br>15<br>13 | | ns | 2.0<br>4.5<br>6.0 | Fig.9 |
| $t_{rem}$ | removal time MR to $CP_U$, $CP_D$ | 50<br>10<br>9 | 0<br>0<br>0 | | 65<br>13<br>11 | | 75<br>15<br>13 | | ns | 2.0<br>4.5<br>6.0 | Fig.10 |
| $t_{su}$ | set-up time $D_n$ to $\overline{PL}$ | 80<br>16<br>14 | 22<br>8<br>6 | | 100<br>20<br>17 | | 120<br>24<br>20 | | ns | 2.0<br>4.5<br>6.0 | Fig.11 note: $CP_U = CP_D$ = HIGH |
| $t_h$ | hold time $D_n$ to $\overline{PL}$ | 0<br>0<br>0 | −14<br>−5<br>−4 | | 0<br>0<br>0 | | 0<br>0<br>0 | | ns | 2.0<br>4.5<br>6.0 | Fig.11 |
| $t_h$ | hold time $CP_U$ to $CP_D$, $CP_D$ to $CP_U$ | 80<br>16<br>8 | 22<br>8<br>6 | | 100<br>20<br>17 | | 120<br>24<br>20 | | ns | 2.0<br>4.5<br>6.0 | Fig.13 |
| $f_{max}$ | maximum up, down clock pulse frequency | 4.0<br>20<br>24 | 13.5<br>41<br>49 | | 3.2<br>16<br>19 | | 2.6<br>13<br>15 | | MHz | 2.0<br>4.5<br>6.0 | Fig.7 |

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: MSI

### Note to HCT types

The value of additional quiescent supply current ($\Delta I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\Delta I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|---|---|
| $D_n$ | 0.35 |
| $\overline{CP}_U$, $CP_D$ | 1.40 |
| $\overline{PL}$ | 0.65 |
| MR | 1.05 |

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}/ t_{PLH}$ | propagation delay $CP_U$, $CP_D$ to $Q_n$ | | 23 | 43 | | 54 | | 65 | ns | 4.5 | Fig.7 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $CP_U$ to $\overline{TC}_U$ | | 15 | 27 | | 34 | | 41 | ns | 4.5 | Fig.8 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $CP_D$ to $\overline{TC}_D$ | | 15 | 27 | | 34 | | 41 | ns | 4.5 | Fig.8 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $\overline{PL}$ to $Q_n$ | | 26 | 46 | | 58 | | 69 | ns | 4.5 | Fig.9 |
| $t_{PHL}$ | propagation delay MR to $Q_n$ | | 22 | 40 | | 50 | | 60 | ns | 4.5 | Fig.10 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $D_n$ to $Q_n$ | | 27 | 46 | | 58 | | 69 | ns | 4.5 | Fig.9 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $\overline{PL}$ to $\overline{TC}_U$, $\overline{PL}$ to $\overline{TC}_D$ | | 31 | 55 | | 69 | | 83 | ns | 4.5 | Fig.12 |
| $t_{PHL}/ t_{PLH}$ | propagation delay MR to $\overline{TC}_U$, MR to $\overline{TC}_D$ | | 29 | 55 | | 69 | | 83 | ns | 4.5 | Fig.12 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $D_n$ to $\overline{TC}_U$, $D_n$ to $\overline{TC}_D$ | | 32 | 58 | | 73 | | 87 | ns | 4.5 | Fig.12 |
| $t_{THL}/ t_{TLH}$ | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.10 |
| $t_W$ | up, down clock pulse width HIGH or LOW | 25 | 11 | | 31 | | 38 | | ns | 4.5 | Fig.7 |
| $t_W$ | master reset pulse width HIGH | 20 | 7 | | 25 | | 30 | | ns | 4.5 | Fig.10 |
| $t_W$ | parallel load pulse width LOW | 20 | 8 | | 25 | | 30 | | ns | 4.5 | Fig.9 |
| $t_{rem}$ | removal time $\overline{PL}$ to $CP_U$, $CP_D$ | 10 | 2 | | 13 | | 15 | | ns | 4.5 | Fig.9 |
| $t_{rem}$ | removal time MR to $CP_U$, $CP_D$ | 10 | 0 | | 13 | | 15 | | ns | 4.5 | Fig.10 |
| $t_{su}$ | set-up time $D_n$ to $\overline{PL}$ | 16 | 8 | | 20 | | 24 | | ns | 4.5 | Fig.11 note: $CP_U = CP_D$ = HIGH |
| $t_h$ | hold time $D_n$ to $\overline{PL}$ | 0 | −6 | | 0 | | 0 | | ns | 4.5 | Fig.11 |
| $t_h$ | hold time $CP_U$ to $CP_D$, $CP_D$ to $CP_U$ | 16 | 7 | | 20 | | 24 | | ns | 4.5 | Fig.13 |
| $f_{max}$ | maximum up, down clock pulse frequency | 20 | 43 | | 16 | | 13 | | MHz | 4.5 | Fig.7 |

## AC WAVEFORMS

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3V; $V_I$ = GND to 3 V.

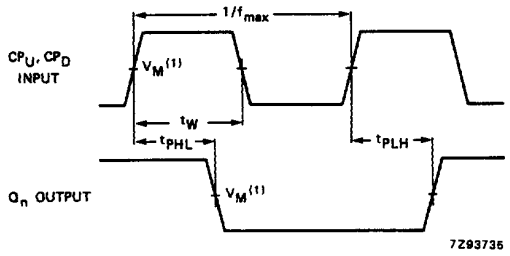


Fig.7 Waveforms showing the clock ($CP_U$, $CP_D$) to output ($Q_n$) propagation delays, the clock pulse width, and the maximum clock pulse frequency.

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3V; $V_I$ = GND to 3 V.

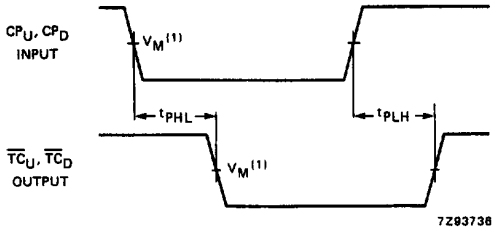


Fig.8 Waveforms showing the clock ($CP_U$, $CP_D$) to terminal count output ($\overline{TC}_U$, $\overline{TC}_D$) propagation delays.

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3V; $V_I$ = GND to 3 V.

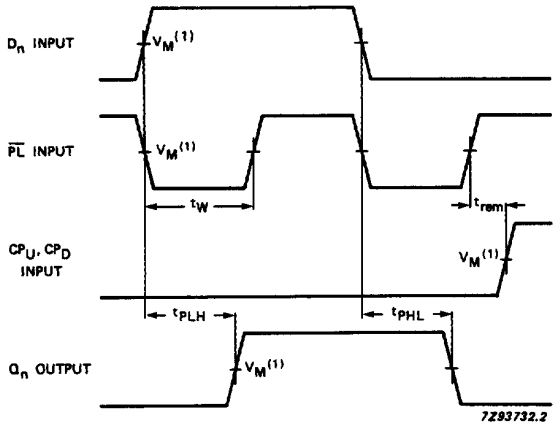


Fig.9 Waveforms showing the parallel load input ($\overline{PL}$) and data ($D_n$) to $Q_n$ output propagation delays and $\overline{PL}$ removal time to clock input ($CP_U$, $CP_D$).

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3V; $V_I$ = GND to 3 V.

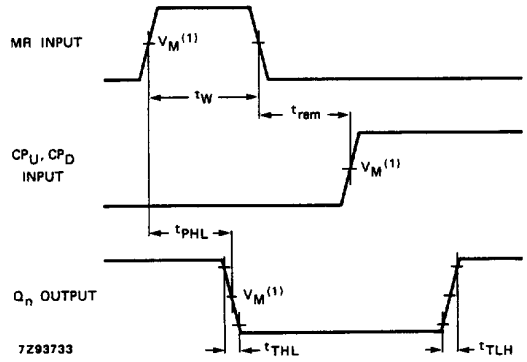


Fig.10 Waveforms showing the master reset input (MR) pulse width, MR to $Q_n$ propagation delays, MR to $CP_U$, $CP_D$ removal time and output transition times.

The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3V; $V_I$ = GND to 3 V.

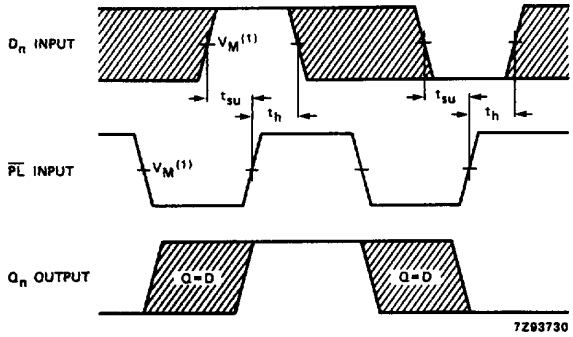


Fig.11 Waveforms showing the data input ($D_n$) to parallel load input ($\overline{PL}$) set-up and hold times.

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3V; $V_I$ = GND to 3 V.

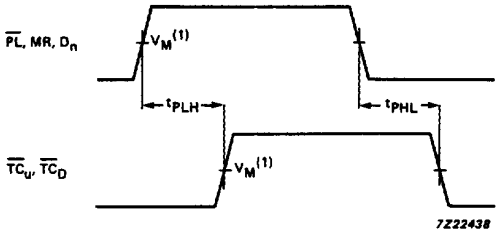


Fig.12 Waveforms showing the data input ($D_n$), parallel load input ($\overline{PL}$) and the master reset input (MR) to the terminal count outputs ($\overline{TC}_U$, $\overline{TC}_D$) propagation delays.

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3V; $V_I$ = GND to 3 V.

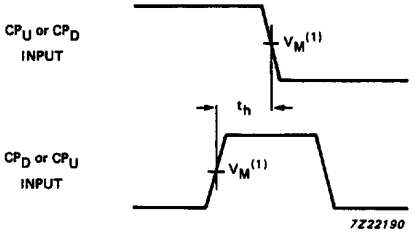


Fig.13 Waveforms showing the $CP_U$ to $CP_D$ or $CP_D$ to $CP_U$ hold times.

## APPLICATION INFORMATION

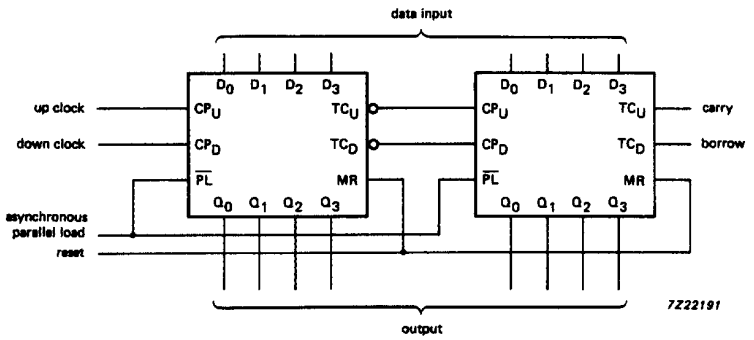


Fig.14 Cascaded up/down counter with parallel load.

## PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.